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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,492	12/05/2003	Eric Hung	03-1237 (5201-27600)	9752

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EXAMINER
BAE, JI H

ART UNIT	PAPER NUMBER
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,492	HUNG ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-29-05, 6-15-05, 7-15-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 11 recites an electronic system "wherein the execution engine, the memory controller, and the memory device comprise a packaged integrated circuit having a plurality of leads extending therefrom." Applicant's specification teaches that the execution engine and the memory controller may comprise a single, packaged integrated circuit, but does not teach that the memory devices are also integrated with the execution engine and memory controller. Fig. 2 and 3 clearly show the system-on-chip comprising the execution engine and the memory controller only. Additionally, pp. 6-7 of applicant's specification teach that only the memory controller and execution engine reside on the same integrated circuit [pp. 6, second paragraph, pp. 7, last paragraph].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keskar et al., U.S. Patent No. 6,366,989 B1, in view of Micron ("Micron Technical Note: General DDR SDRAM Functionality", Micron Technology Inc Technical Note)[1].

Regarding claim 1, Keskar teaches an integrated circuit comprising [Fig. 2]:

an execution engine clocked at a first clock rate [CPU 22];

a memory controller clocked at a second clock rate less than the first clock rate [SDC 30, memory interface 66]; and

a plurality of pins adapted to transfer data to and from the memory controller [data lines 84].

Keskar teaches that the memory interface operates at a clock speed which is slower than that of the CPU [col. 3, lines 55-59]. Keskar does not teach that the data transfer between memory interface and memory devices occurs on both the rising and falling edges of the second clock.

Micron teaches that DDR memory improves over SDR memory by causing data to be transmitted at twice the rate of the clock frequency [page 1, Introduction, first and second paragraphs]. Micron teaches that this is accomplished by sending data on both the positive and negative clock edges [page 2, second column, second paragraph].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar and Micron by implementing the memory controller of Keskar to work with DDR SDRAMs, as taught by Micron. The disclosure of Keskar teaches that the memory controller interfaces with an SDRAM array [array 40, Fig. 2]. Micron teaches that DDR SDRAMs represent an improvement over SDR SDRAMs by allowing data to be transmitted at a faster

rate. Therefore, the teachings of Micron would improve the system of Keskar by allowing Keskar to be used with devices that provide a faster data transmission rate.

Regarding claim 4, Micron teaches that the DDR SDRAMs utilize a true and complementary clock [page 2, second column, third paragraph].

Regarding claim 7, Micron teaches the memory controller receives a power supply voltage of 1.25 V [page 10, I/O Signaling, first column, first paragraph].

Regarding claim 21, Keskar and Micron teach:

integrating an execution engine with a memory controller [Keskar, col. 2, lines 11-14];

clocking the execution engine with a first clock that cycles at a first clock rate;

clocking the memory controller with a second clock that cycles at a second clock rate less than the first clock rate [Keskar, col. 3, lines 55-59];

clocking a memory device, formed separate and apart from the integrated execution engine and memory controller, with the second clock; and

transferring data between the memory controller and the memory device at both the leading and trailing edge of the second clock [Micron, page 2, second column, second paragraph].

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keskar in view of Micron as applied to claim 1 above, and further in view of Bolken, U.S. Patent No. 6,955,941 B2.

Regarding 8, Keskar/Micron teaches the limitations of claim 1, but does not teach a plurality of bonding pads wire bonded to corresponding leads from the integrated circuit.

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[1] Applicant-cited reference

Bolken teaches a packaging for an integrated circuit wherein bond pads of the integrated circuit are wire bonded to a lead frame [col. 3, lines 15-37].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Bolken with that of Keskar/Micron. Keskar/Micron disclose an integrated circuit, but do not teach a packaging for the integrated circuit. The teachings of Bolken would improve the system of Keskar/Micron by providing a packaging that increases the integrated circuit density [col. 2, lines 58-63].

Claims 9, 10, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keskar in view of Micron in view of Holm [Eirik Holm, "The Printed Circuit Board Primer" retrieved from the Internet at http://www.tomshardware.com/2001/08/10/the_printed_circuit_board_primer/] in view of Chen et al., U.S. Patent No. 6,320,758 B1.

Regarding claim 9, Keskar teaches [Fig. 2]:

an execution engine adapted to receive a first clock signal [CPU 22];

a memory controller adapted to receive a second clock signal with frequency less than the first clock signal [SDC 30, memory interface 66];

a memory device comprising an array of DRAM cells [SDRAM array 40];

a data bus transferring data between the memory controller and memory device [address/data/control lines 80, 82, 84].

Keskar does not teach transferring data at twice the rate of the second clock.

Micron teaches that DDR memory improves over SDR memory by causing data to be transmitted at twice the rate of the clock frequency [page 1, Introduction, first and second

paragraphs]. Micron teaches that this is accomplished by sending data on both the positive and negative clock edges [page 2, second column, second paragraph].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Keskar and Micron by implementing the memory controller of Keskar to work with DDR SDRAMs, as taught by Micron. The disclosure of Keskar teaches that the memory controller interfaces with an SDRAM array [array 40, Fig. 2]. Micron teaches that DDR SDRAMs represent an improvement over SDR SDRAMs by allowing data to be transmitted at a faster rate. Therefore, the teachings of Micron would improve the system of Keskar by allowing Keskar to be used with devices that provide a faster data transmission rate.

Keskar/Micron does not teach a substrate comprising several layers, with conductors extending partially across the layers, with components coupled to the conductors.

Holm teaches that printed circuit boards comprise:

a substrate comprising a plurality of conductive layers spaced from each other by a dielectric layer ["Multi-Layer Boards", page 1, first paragraph];

a plurality of conductors extending partially across one of the conductive layers, with components coupled to the conductors ["What is a PCB?", page 2, conductor pattern w/electrical connections, "What is a PCB? Continued", page 1, first paragraph].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Holm with Keskar/Micron by mounting the execution engine, memory controller, and memory devices on a printed circuit board, such as the one taught by Holm. PCBs are old and well-known in the art, and are conventionally used in electronic devices to mount components and provide the necessary connectivity between them. Holm teaches ["What is a PCB?", page 1, second paragraph]:

"A PCB is found in almost every electronic device. If you have electronic components in a device, they are mounted on a PCB, big or small. Besides keeping the components in place, its purpose of a PCB is to provide electrical connections between the components mounted on it."

Keskar/Micron/Holm does not teach that the PCB comprises a maximum of two layers.

Chen teaches a PCB with only two layers [col. 3, lines 60-61]. It would have been obvious to one of ordinary skill in the art to combine the teachings of Chen with those of Keskar/Micron by implementing the circuit of Keskar/Micron in a PCB comprised of two layers, as taught by Chen. Holm teaches that PCBs with fewer layers result in decreased manufacturing costs ["Where the Cost Savings Come In", page 2]. The teachings of Chen would provide an improvement over Keskar/Micron by providing a way to realize this cost reduction.

Regarding claim 9, although Keskar/Micron/Holm/Chen teaches that the data is transferred at twice the memory controller clock rate, it is not explicitly taught that the 2x rate of the memory controller clock is greater than the processor clock rate [first clock rate]. However, the clock rates would have been obvious as a matter of design choice. Kozierok teaches that processors typically multiply memory bus speeds by an array of multiplier values [Charles Kozierok, "Processor Speed Support", retrieved from the Internet at http://www.pcguide.com/ref/mbsys/chip/func/cpuSpeed-c.html].

Regarding claim 10, 14, and 15, Holm teaches that:

one of the conductive layers resides on an outer surface of the board ["What is a PCB?", page 2, conductor pattern];

devices are mounted on an outer surface of the substrate ["What is a PCB?", page 2, components mounted on PCB];

that the conductive layers comprise copper ["What is a PCB?", page 2, copper foil].

Regarding claim 16, Holm teaches that the dielectric layer comprises epoxy-bonded fiberglass ["Manufacturing Process", page 1, first paragraph, glass epoxy].

Regarding claim 17, Holm teaches that a via couples two conductive layers ["Double Sided Boards", page 4, vias].

Regarding claims 18 and 19, Micron teaches SSTL termination with a pull-up resistor, the pull-up voltage having a value of 1.25 volts [page 10, I/O Signaling, first column, first paragraph].

Claims 11-13 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keskar/Micron/Holm/Chen as applied to claim 9 above, and further in view of Bolken.

Regarding claim 11, Keskar/Micron/Holm/Chen does not teach a packaged integrated circuit.

Bolken teaches a packaged integrated circuit having a plurality of leads extending therefrom [Fig. 1].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Bolken with that of Keskar/Micron/Holm/Chen. Keskar/Micron/Holm/Chen disclose an integrated circuit, but do not teach a packaging for the integrated circuit. The teachings of Bolken would improve the system of Keskar/Micron by providing a packaging that increases the integrated circuit density [col. 2, lines 58-63].

Regarding claim 12, Bolken teaches bonding pads and a lead frame having bonding fingers, with wires solder coupled between bonding pads and bonding fingers [col. 3, lines 15-37].

Regarding claim 13, Holm teaches a set of solder pads to which leads are solder coupled ["Component Mounting and Soldering", page 1].

Regarding claim 20, Bolken teaches a TSOP packaging [col. 3, lines 1-5].

Regarding claim 21, Keskar and Micron teach:

integrating an execution engine with a memory controller [Keskar, col. 2, lines 11-14];

clocking the execution engine with a first clock that cycles at a first clock rate;

clocking the memory controller with a second clock that cycles at a second clock rate less than the first clock rate [Keskar, col. 3, lines 55-59];

clocking a memory device, formed separate and apart from the integrated execution engine and memory controller, with the second clock; and

transferring data between the memory controller and the memory device at both the leading and trailing edge of the second clock [Micron, page 2, second column, second paragraph].

Regarding claim 22, Keskar/Micron/Holm/Chen/Bolken teaches:

packaging the integrated circuits;

coupling the circuits to a PCB;

wherein the PCB comprises two conductive layers spaced apart by a dielectric layer.

Regarding claims 23 and 24, Micron teaches SSTL termination with a pull-up resistor, the pull-up voltage having a value of 1.25 volts [page 10, I/O Signaling, first column, first paragraph].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Fulcher, U.S. Patent No. 5,686,764;

Rajan et al., U.S. Patent No. 6,781,405 B2;

Lelm et al., U.S. Patent No. 5,448,715;

Samson et al., U.S. Patent No. 6,971,034 B2;

Dorst, U.S. Patent No. 6,941,416 B2;

Fischer et al., U.S. Patent No. 5,239,639;

Chua-Eoan et al., U.S. Patent No. 2003/0217303 A1;

Chiu, U.S. Patent No. 6,603,828 B1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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